CLAIMS

1. A method of evaluating performance of a test environment and an actual electronic device during testing of the electronic device, said method comprising:

creating a virtual test environment emulating an actual test environment in which the electronic device is to be tested;

implanting a virtual device emulating the actual electronic device into the virtual test environment;

stimulating the virtual device with an input test signal emulating an actual input signal to be applied to the actual electronic device during testing; and

evaluating the integrity of the input test signal and a resulting output signal from the virtual device.

2. A method as claimed in claim 1, further comprising performing a virtual calibration of the virtual test environment.

3. A method as claimed in claim 2, further comprising improving the virtual calibration based on the evaluation.

4. A method as claimed in claim 1, further comprising performing a virtual adjustment of the virtual device based on the evaluation.

5. A method as claimed in claim 1, further comprising improving the design of the actual electronic device based on the environment.

6. An article, comprising a storage medium having instructions stored thereon, the instructions when executed evaluating performance of a test environment and of an actual electronic device during testing of the electronic device by creating a virtual test environment

emulating an actual test environment in which the electronic device is to be tested; implanting a virtual device emulating the actual electronic device into the virtual test environment; stimulating the virtual device with an input test signal emulating an actual input signal to be applied to the actual electronic device during testing; and evaluating the integrity of the input test signal and a resulting output signal from the virtual device.

7. An article as claimed in claim 6, wherein the instructions when executed additionally perform a virtual calibration of the virtual test environment.

8. An article as claimed in claim 7, wherein the instructions when executed additionally improve the virtual calibration based on the evaluation.

9. An article as claimed in claim 6, wherein the instructions when executed additionally perform a virtual adjustment of the virtual device based on the evaluation.

10. An article as claimed in claim 6, wherein the instructions when executed additionally improve the design of the actual device based on the evaluation.

11. Apparatus for evaluating the performance of a test environment and of an actual electronic device, said apparatus comprising:

a virtual device emulating the actual electronic device;

a virtual test environment, emulating an actual test environment in which the electronic device is to be tested, to apply to said virtual device an input test signal emulating an actual input signal to be applied to the actual electronic device during testing; and

timing circuitry to evaluate the integrity of the input test signal and a resulting output signal from the virtual device.

12. Apparatus as claimed in claim 11, wherein said virtual test environment emulates a general purpose tester and a tester interface unit specific to the electronic device.

13. Apparatus as claimed in claim 12, wherein said timing circuitry comprises a first timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device.

14. Apparatus as claimed in claim 11, wherein said virtual test environment comprises a virtual test driver to apply the input test signal to said virtual device, and a virtual test receiver to receive the output test signal from said virtual device.

15. Apparatus as claimed in claim 14, wherein said timing circuitry comprises a first timer to determine the time interval between output of the input test signal by said virtual test driver and receipt of the output test signal by said virtual test receiver, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device.

16. Apparatus as claimed in claim 11, wherein said timing circuitry comprises a first timer to determine the time interval between output of the input test signal by said virtual test environment and receipt of the output test signal by said virtual test environment, and a second timer to determine the time interval between receipt of the input test signal by said virtual device and output of the output test signal by said virtual device.

17. Apparatus as claimed in claim 11, comprising a general purpose processing system.